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M.Tech. Degree Examination, Dec.2014/Jan.2015
Low Power VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

- 1 a. Explain the CMOS leakage currents. (08 Marks)
b. What are basic principles of low power design? (08 Marks)
c. Draw the energy band diagram of an unbiased MIS diode. (04 Marks)
- 2 a. With usual notations show that the short circuit power dissipation in a CMOS inverter is given by, $P_{SC} = \frac{\beta}{12} (V_{DD} - V_{th})^3 \frac{\tau}{T}$. (08 Marks)
b. Explain the merits and demerits of SPICE power analysis. (08 Marks)
c. Explain how to calculate the internal switching energy. (04 Marks)
- 3 a. Explain the steps involved in event driven gate level power simulation. (06 Marks)
b. Explain the architectural level power model based on activities. (08 Marks)
c. Explain Monte-Carlo simulation. Derive the expression for number of sample to stop simulation. (06 Marks)
- 4 a. Along with expression, explain word-level and bit-level statistics. (08 Marks)
b. If P(a), P(b) and P(c) are input static probabilities, find the output static probability of $y = ab+c$ by using Shannon's decomposition method. (08 Marks)
c. Define signal entropy. (04 Marks)
- 5 a. Explain sizing an inverter chain with relevant figures and expressions. (10 Marks)
b. Explain transistor network restructuring. (10 Marks)
- 6 a. Explain Bus invert encoding with suitable diagram. (10 Marks)
b. Explain transition analysis of state encoding with example. (10 Marks)
- 7 a. Explain basics of precomputation logic with example. (10 Marks)
b. What are design issues in precomputation logic techniques? (10 Marks)
- 8 Write short notes on:
a. Low power bus.
b. Charge recycling bus.
c. Single driver versus distributed buffers.
d. Design trade offs in state machine encoding. (20 Marks)
